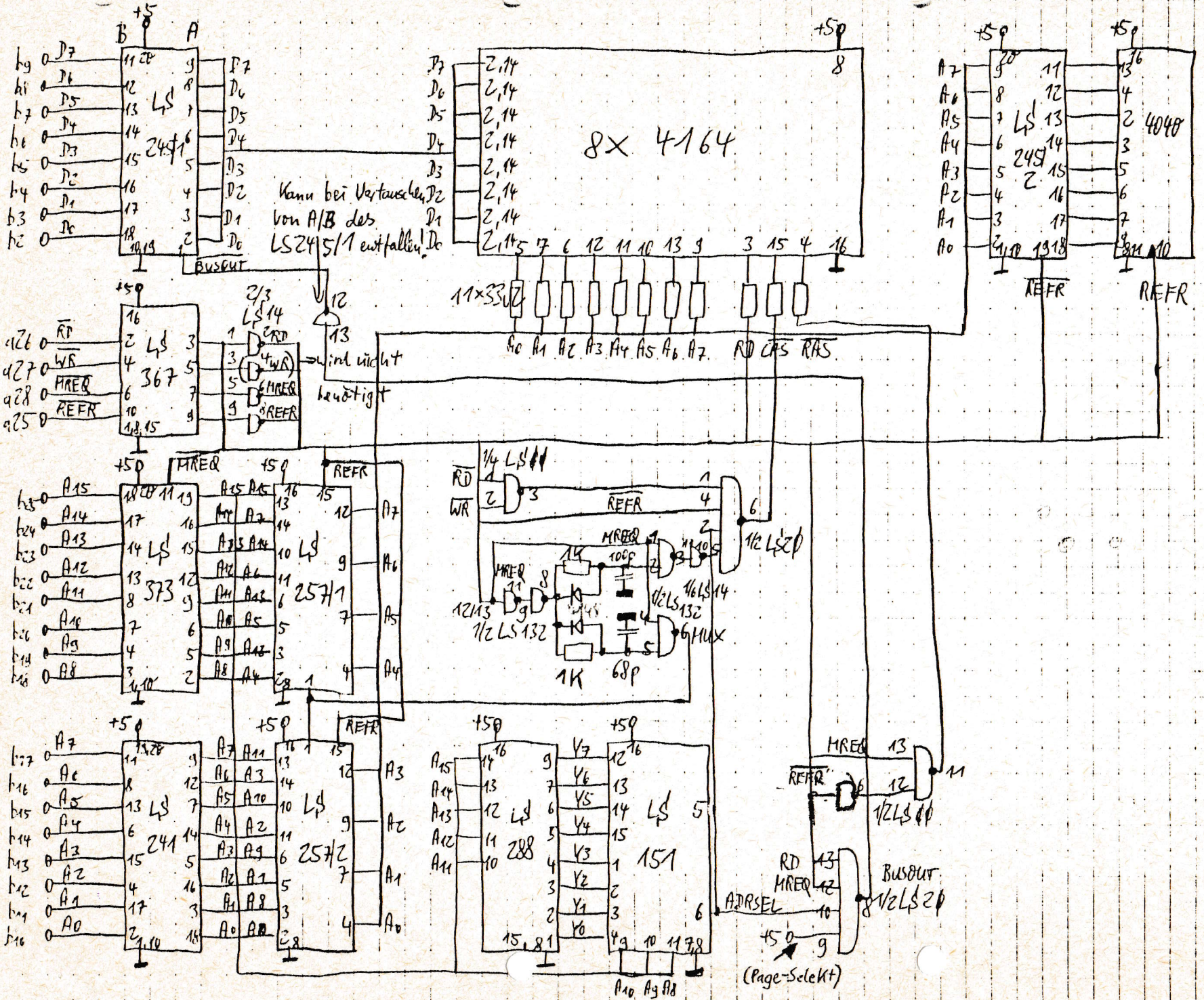
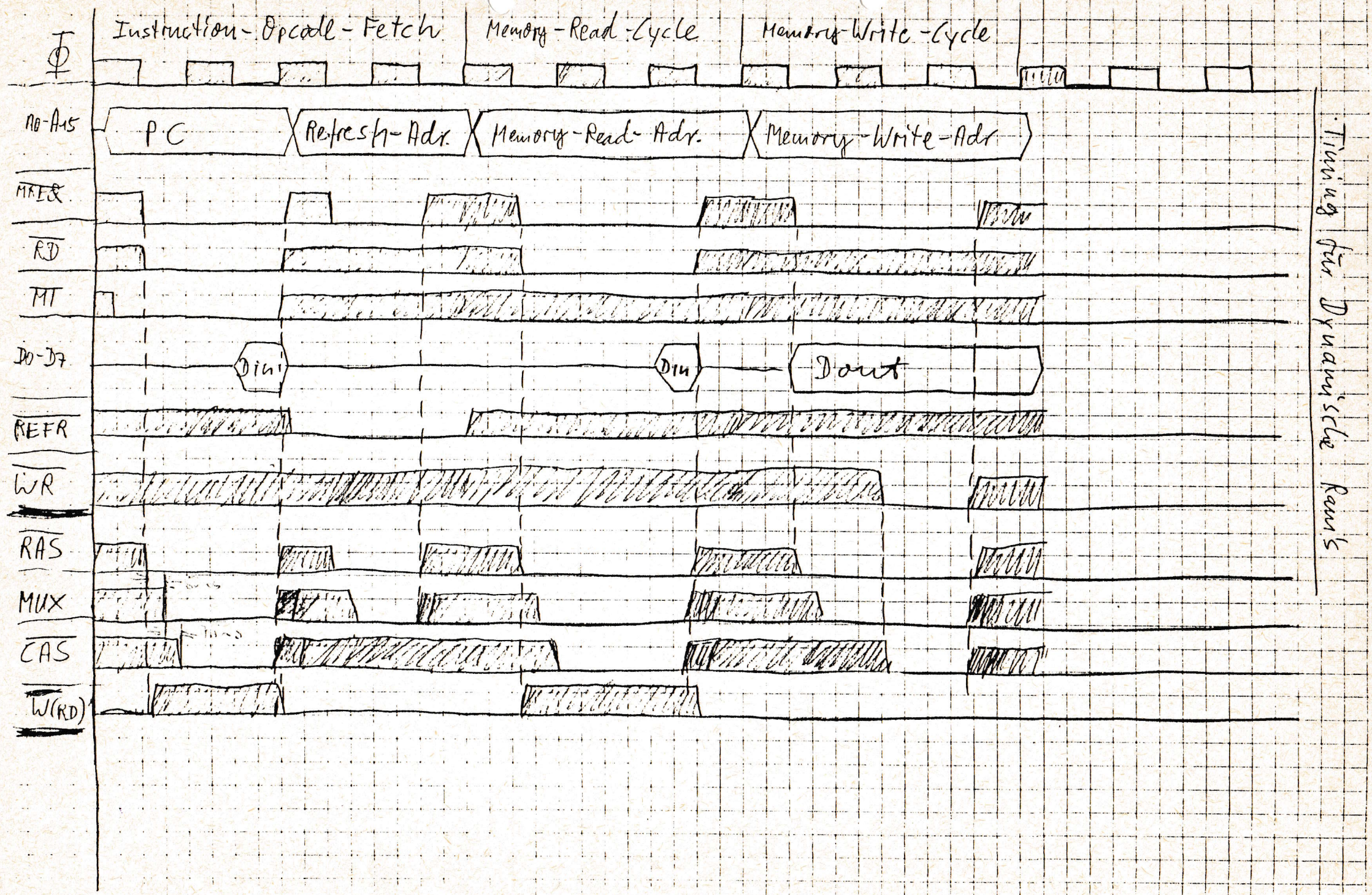
64 K-Byte dyn. RAM für STDE-Bus





Timing für Dynamische Rams

Decodier Prom für dyn. RAM-Karte — LS288

PROM-Adr.	D7	D6	D5	D4	D3	D2	D1	D0	RAM-Bereich
0	0	0	0	0	0	0	0	0	0000 – 07FF
1	0	0	0	0	0	0	0	0	0800 – 0FFF
2	0	0	0	0	1	1	1	1	1000 – 17FF
3	0	0	0	0	0	0	0	0	1800 – 1FFF
4	0	0	0	0	0	0	0	0	2000 – 27FF
5	0	0	0	0	0	0	0	0	2800 – 2FFF
6	0	0	0	0	0	0	0	0	3000 – 37FF
7	0	0	0	0	0	0	0	0	3800 – 3FFF
8	0	0	0	0	0	0	0	0	4000 – 47FF
9	0	0	0	0	0	0	0	0	4800 – 4FFF
10	0	0	0	0	0	0	0	0	5000 – 57FF
11	0	0	0	0	0	0	0	0	5800 – 5FFF
12	0	0	0	0	0	0	0	0	6000 – 67FF
13	0	0	0	0	0	0	0	0	6800 – 6FFF
14	0	0	0	0	0	0	0	0	7000 – 77FF
15	0	0	0	0	0	0	0	0	7800 – 7FFF
16	0	0	0	0	0	0	0	0	8000 – 87FF
17	0	0	0	0	0	0	0	0	8800 – 8FFF
18	0	0	0	0	0	0	0	0	9000 – 97FF
19	0	0	0	0	0	0	0	0	9800 – 9FFF
20	0	0	0	0	0	0	0	0	A000 – A7FF
21	0	0	0	0	0	0	0	0	A800 – AFFF
22	0	0	0	0	0	0	0	0	B000 – B7FF
23	0	0	0	0	0	0	0	0	B800 – BFFF
24	0	0	0	0	0	0	0	0	C000 – C7FF
25	0	0	0	0	0	0	0	0	C800 – CFFF
26	0	0	0	0	0	0	0	0	D000 – D7FF
27	0	0	0	0	0	0	0	0	D800 – DFFF
28	1	1	1	1	1	1	1	1	E000 – E7FF
29	1	1	1	1	1	1	1	1	E800 – EFFF
30	0	0	0	0	0	0	0	0	F000 – F7FF
31	1	1	1	1	1	1	1	1	F800 – FFFF

STECKERLEISTE VG Leiste 2 reihig Serie B

	Masse	a	1	b	1	Masse
	POWER READY	a	2	b	2	D 0
	(– 5V)	a	3	b	3	D 1
	(+ 12 V)	a	4	b	4	D 2
	(– 12 V)	a	5	b	5	D 3
	(+ 15 V)	a	6	b	6	D 4
	(– 15 V)	a	7	b	7	D 5
		a	8	b	8	D 6
		a	9	b	9	D 7
		a	10	b	10	A 0
		a	11	b	11	A 1
		a	12	b	12	A 2
	A 17	a	13	b	13	A 3
	A 16	a	14	b	14	A 4
	$\overline{\text{RESETA}}$	a	15	b	15	A 5
	$\overline{\text{HALT}}$	a	16	b	16	A 6
	IEO	a	17	b	17	A 7
	IEI	a	18	b	18	A 8
	$\overline{\text{INT}}$	a	19	b	19	A 9
	$\overline{\text{NMI}}$	a	20	b	20	A 10
	$\overline{\text{BUSAK}}$	a	21	b	21	A 11
(Hold)	$\overline{\text{BUSRQ}}$	a	22	b	22	A 12
	$\overline{\text{RESET}}$	a	23	b	23	A 13
(Ready)	$\overline{\text{WAIT}}$	a	24	b	24	A 14
	$\overline{\text{RFSH}}$	a	25	b	25	A 15
	$\overline{\text{RD}}$	a	26	b	26	$\overline{\text{MREQ}} \cdot \overline{\text{RD}}$
	$\overline{\text{WR}}$	a	27	b	27	$\overline{\text{MREQ}} \cdot \overline{\text{WR}}$
	$\overline{\text{MREQ}}$	a	28	b	28	Master/Stave
	$\overline{\text{IORQ}}$	a	29	b	29	$\overline{\text{IORQ}} \cdot \overline{\text{WR}}$
	$\overline{\text{M 1}}$	a	30	b	30	$\overline{\text{IORQ}} \cdot \overline{\text{RD}}$
10 MHZ	$\overline{\text{TAKT}}$	a	31	b	31	$\overline{\Phi}$ 2,5 MHZ
	+ 5 V	a	32	b	32	+ 5 V

Datenbus

Adressbus